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Docket No.: 0090-447

PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of

Motoshige IGARASHI, et al.

Serial No.: 09/971,958 : Group Art Unit: 2814

Filed: October 09, 2001 : Examiner: T. N. Quach

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

- ☐ No additional fee is required.
- ☐ Applicant is entitled to small entity status under 37 CFR 1.27
- ☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	11	20	0	$18.00 =	$0.00
Independent Claims	1	3	0	$84.00 =	$0.00
		Multiple claims newly presented			$0.00
		Fee for extension of time			$400.00
					$0.00
				Total of Above Calculations	$400.00

☒ Please charge my Deposit Account No. 500417 in the amount of $400.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Date: October 22, 2002

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Motoshige IGARASHI, et al.	:	
Application No.: 09/971,958	:	Group Art Unit: 2814
Filed: October 9, 2001	:	Examiner: T. Quach

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

AMENDMENT

Box Fee Amendment
The Commissioner for Patents and Trademarks
Washington, DC 20231

Sir:

The following Amendment and Remarks are submitted in response to the Office Action dated May 23, 2002. Please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claim 1 as follows:

Sub A1 B1

1. (Amended) A semiconductor device comprising:

a gate electrode formed on a semiconductor substrate through a gate insulating film;

a pair of impurity diffusion layers formed on the surface region of said semiconductor substrate at both sides of said gate electrode; and

a first insulating film formed so as to cover the sidewalls of said gate electrode, and to extend to the surface area of a specific range of said semiconductor substrate only in the vicinity of